REMARKS

Reconsideration is respectfully requested in view of any changes to the claims and the remarks herein. Please contact the undersigned to conduct a telephone interview in accordance with MPEP 713.01 to resolve any remaining requirements and/or issues prior to sending another Office Action. Relevant portions of MPEP 713.01 are included on the signature page of this amendment.

References to Applicants' specification will be by referring to the column and line number from issued parent patent US 5,706,067.

Objections to the Specification

The specification has been objected to "as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o)." Applicants respectfully disagree.

The Examiner states:

> The combination of a mirror with the first electrode over the switching device and the capacitor, and any reference to a frame in respect to the first electrode, or a blocking layer below it.

Applicants respectfully disagree. Applicants teach throughout the specification, in particular, in original claim 1, circuits in a semiconductor substrate, with liquid crystal device (spacial light modulator) over the substrate. The circuit is the switching device. The liquid crystal device includes electrodes, in particular original claim 8 teaches spacial light modulator having an electrode. Original claim 12 teaches that the spacial light modulator has a capacitor. The frame is the edge of the electrode.

The specification teaches at column 9, lines 26-43:

> A spatial light modulator array based on a reflective liquid crystal..... The array comprises a plurality of liquid crystal devices positioned over respective mirrors on a dielectric layer on a semiconductor

> substrate, a plurality of electrical circuits formed in the semiconductor substrate ... and a reflector/absorber layer positioned and patterned with respect to the mirrors for shielding or blocking light from passing into the semiconductor substrate containing the electrical circuits, the reflector/absorber layer having **an edge overlapping an edge of the mirror to form an overlapping region to decrease ambient light from passing into the semiconductor substrate** and to provide **a capacitor** for maintaining a voltage on the mirror which functions as the bottom electrode of the respective liquid crystal device. (Emphasis added.)

The examiner further states "The specification shows a single pixel electrode 30 as the mirror, which means that the pixel electrode cannot be construed as the first electrode, as it is already recited in the claims as the mirror." Applicants respectfully disagree. Applicants claim language does not preclude the mirror and first electrode from being the same element. At page 6, lines 13-17 applicants teach "Liquid crystal device 12 comprises a liquid crystal material 26, a top electrode 28 which may be for example In-Sn oxide (ITO), a bottom electrode/mirror 30 which functions as an electrode and a mirror." Thus the Examiner's conclusion that "[t]herefore, the first electrode would have to be some electrode below the pixel, such as the electrode 22" is mere conjecture on the part of the Examiner.

The Examiner further states "The electrodes below the pixel are not shown in the specification or the figures to have the transistor below them." Applicants respectfully disagree. In the sentence bridging pages 1 and 2 applicants teach "With single crystal Si transistors, the transistor switching speeds are faster than with amorphous-Si or polycrystalline Si transistors now used for flat panel displays." The transistors are in the substrate 14, preferable silicon, and the mirrors are above the substrate. Thus applicants disagree with the Examiner's statement "[a]lthough the transistor must be in the semiconductor layer, it need not be below any of the layers connecting the pixel to the transistor itself."

The Examiner further states:

> "Further, most of the layers construable as the first electrode lack an absorbing layer below them, or an element which can be considered a

"frame" around them, and particularly not an opaque frame. See Appendix 1, which compares an LCD as claimed with the LCD devices disclosed in the specification.

As stated above applicants teach electrodes 28 and 30 which are shown in Fig. 1 to be above reflector/absorber layer 34. In appendix 1 the Examiner marks an element of applicants Fig. 1 as a "pixel electrode". Applicants do not refer to this element as a "pixel electrode". Applicants' original claim 2 recites "The spatial light modulator array of claim 1 wherein said reflector/absorber layer overlaps said edge of said mirror." The US 5,652,667 teaches in claim 4 "a frame composition disposed along an edge of said first electrode, with said frame composition being composed of optical blocking insulating material for blocking incident light from leaking into said switching element ... an optical reflector formed on said first electrode." The abstract of US 5,652,667 teaches "A first electrode 2."

As stated above applicants teach "electrode/mirror 30 which functions as an electrode and a mirror." Thus applicants teach that the reflector/absorber layer overlaps the edge of an electrode" and applicants abstract teaches "a reflector/absorber layer for blocking light."

Interference

The Examiner states:

Claim 77 of this application has been copied from U.S. Patent No. 5708486 and claims 57-63 and 67-70, 71 of this application has been copied from U.S. Patent No, 5708486 for the purpose of an interference. Applicant has failed to specifically apply each limitation or element of each of the copied claim(s) to the disclosure of the application. Applicant is required to show how applicant believes each limitation or element is supported in the specification.

The text of CLAIM 77 is:

A display unit comprising:

a first substrate comprising a plurality of reflection electrodes with a gap portion formed therebetween, a second substrate opposing said first substrate having a transparent electrode, and a liquid crystal material being put between said first and said second substrates, wherein said first substrate has a shading layer at least part of said gap portion and wherein said shading layer exhibits a different reflection characteristic from said reflection electrodes, said shading layer comprises an anti-reflection surface.

Support in the specification for claim 77 is as given the table below.

Claim 77	**Support in specification**
A display unit comprising	The field of the invention states "This invention relates to display devices"
a first substrate comprising a plurality of reflection electrodes	Original Claim 1 recites: "a plurality of liquid crystal devices positioned ... on a semiconductor substrate"} with a gap portion formed therebetween,
with a gap portion formed therebetween,	"FIG. 11 shows a scanning electron micrograph of an array 11 of spatial light modulators 10" Spacial light modulator is shown in Fig. 10 and gap between the elements 24, 36 of the spacial light modulator 10"
a second substrate opposing said first substrate having a transparent electrode,	("A liquid crystal device 12 is shown positioned over substrate 14 which may be a single crystal semiconductor. " Substrate 14 is the first substrate.)
and a liquid crystal material being put between said first and said second substrates	"Liquid crystal device 12 comprises a liquid crystal material 26, a top electrode 28 which may be for example In-Sn oxide (ITO)." ITO is the transparent second substrate.
wherein said first substrate has a shading layer at least part of said gap portion and wherein said shading layer exhibits a different reflection characteristic from said reflection electrodes, said shading layer comprises an anti-reflection surface	.("A reflector/absorber layer 34 functions to block or attenuate ambient light and impinging light on spatial light modulator 10 and passing through openings or gaps 56 between mirrors such as bottom electrode/mirror 33 and bottom electrode mirror 30 shown by arrows 54, 58 and 59 from passing into semiconductor substrate 14.")

The Examiner further states:

> Claim 77 of this application is asserted by applicant in page 2 of paper #20 to correspond to claim(s) of U.S. Patent No. 5,708,486. The examiner does not consider this claim to be directed to the same invention as that of U.S. Patent No. 5,708,486 because the term "reflection characteristics" as employed in the specification of the patent is used in a different sense then the term used in the specification of the instant application.

The Examiner does not support this statement by reference to US 5,708,486 or to the present specification. Applicants disagree with the Examiner's statement. As stated by Applicants in paper #20 claim 77 is substantially the same within the meaning required to establish an interference-in-fact.

The Examiner further states:

> The term reflection characteristics has ambiguity in that every two things have different characteristics of some sort as the set of what can be construed is essentially open. The context of the specification sets forth the characteristics that are referred.

The Examiner does not specifically identify what specification is being referred to in the language "the context of the specification". Applicants request the Examiner to clarify to which specification the Examiner is referring: to Applicants', or to that of US 5,708,486.

The Examiner further states:

> The general use is in optical areas is the distribution of light off of a surface, and this is the use clearly established in the specification of the patent. The use in the instant application is less clear and the term has therefore been rejected as indefinite.

Applicants disagree that term "reflection characteristics" is indefinite in the instant application. Gap region 56 of Fig. 1 of the instant application has a different reflection characteristic than the reflection electrodes 30.

The Examiner further states:

> If a meaning of the term can be established, it appears that it would be the ratio of reflection to absorption, a meaning which is clearly distinct from the meaning employed by the patent. Accordingly, an interference cannot be initiated based upon this claim.

Applicants respectfully disagrees. The Examiner does not specifically state which "patent" is being referenced.

Whether an interference in fact exists is determined according to 37 CFR 1.601 which states:

> i) An interference is a proceeding instituted in the Patent and Trademark Office before the Board to determine any question of patentability and priority of invention between two or more parties **claiming the same patentable invention**. (emphasis added.)

Thus whether there is an interference is determined by the "claimed invention."

37 CFR 1.601 further states:

> (j) "An interference-in-fact exists when at least **one claim** of a party that is designated to correspond to a count and at least **one claim** of an opponent that is designated to correspond to the count **define the same patentable invention**." (Emphasis added.)

Thus the claims are compared to determine if there is an interference-in-fact.

37 CFR 1.601 further states:

> "(n) Invention "A" is the same patentable invention as an invention "B" when invention "A" is the same as (35 U.S.C. 102) or is obvious (35 U.S.C. 103)) in view of invention "B" assuming invention "B" is prior art with respect to invention "A". Invention "A" is a separate patentable invention with respect to invention "B" when invention "A" is new (35 U.S.C. 102) and non-obvious (35 U.S.C. 103) in view of invention "B" assuming invention "B" is prior art with respect to invention "A".

Thus the claims are compared to determine if there is an interfernce-in-fact. There is no provision in 37 CFR 1.601 for a term in a claim to be given a narrower meaning than the literal claim term meaning based on an interpretation from the specification as the Examiner is doing the present prosecution. Thus the Examiner's analysis is inconsistent with the Rules of Practice.

The Examiner further states:

> Claim 57-63 and 67-70, 71 (77) of this application is asserted by applicant in page 2 of paper #20 to correspond to claim(s) of U.S. Patent No. 5,652,667. The examiner does not consider this claim to be directed to the same invention as that of U.S. Patent No. 5,652,667 because the specification of the instant application lacks support of the claimed limitations including:
> The transistor and capacitor below the first electrode.
> First electrode having an opaque frame.
> The first electrode having a frame, and an opaque layer below it.

Applicants respectfully disagree. Applicants transistor is below liquid crystal device 12 of Applicants' Fig. 1. Applicants teach at Col. 2, line 59, to Col. 3, line 13:

> A liquid crystal device 12 is shown positioned over substrate 14, which may be a single crystal semiconductor or semiconductor on insulator (SOI) such as Si or SiGe, containing a plurality of electrical circuits 16 (not shown) which are connected by interlevel vias (such as via or stud 17), polysilicon layers 18 and 20, and metal layer 22.

Applicants teach a capacitor below the first electrode. Applicants teach at Col. 3, lines 34-39:

> Capacitor 48 is coupled (interconnections are not shown) with capacitor 50 formed by polysilicon layer 18, dielectric layer 38 and polysilicon layer 20 which functions to hold the voltage on electrode/mirror 30.

Both capacitors 48 and 50 are below 28 and 30 as shown in Fig. 1.

Applicants further teach at Col. 1, lines 24-30:

> With single crystal Si transistors, the transistor switching speeds are faster than with amorphous-Si or polycrystalline Si transistors now used for flat panel displays and would permit displays with a higher frame rate and higher information content. Additionally, even older Si chip manufacturing facilities can support much finer feature sizes on a SLM than are available with current flat panel manufacturing technology

Thus Applicants teach an electrode with a frame.

US 5652667 to Kurogane teaches at Col. 4, lines, 23-25:

> The edge of the pixel electrode 2, which is a frame 21, is filled up with a silicon dioxide insulating film.

Applicants teach at col. 3, lines 8-12:

> A reflector/absorber layer 34 functions to block or attenuate ambient light and impinging light on spatial light modulator 10 and passing through openings or gaps 56 between mirrors such as bottom electrode/mirror 33 and bottom electrode mirror 30.

Applicants teach at Col. 2, lines 25-29:

> The reflector/absorber layer provides optical shielding for the plurality of electrical circuits from ambient and the impinging light, the reflector/absorber layer having an edge overlapping an edge of the mirror.

Thus Applicants' frame and the frame of US 5652667 to Kurogane are the same.

The Examiner further states "Further, the use of the term "frame" as employed in the current claims is indefinite." Applicants respectfully disagree. The Examiner provides no explanation of this comment. Thus, an interference can be initiated based upon these claims.

Claim Rejections - 35 USC § 112

Claims 47- 61, 80-91, 108-109,111-118,132-133 have been "rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention." Applicants respectfully disagree.

Applicants do not understand the point that the Examiner is making by the following sentence:

> The combination of a mirror with the first electrode over the switching device and the capacitor, and any reference to a frame in respect to the first electrode, or a blocking layer below it.

The Examiner further states:

> The specification shows a single pixel electrode 30 as the mirror, which means that the pixel electrode cannot be construed as the first electrode, as it is already recited in the claims as the mirror.

Applicants respectfully disagree. The pixel electrode can function as a mirror and a first electrode. Moreover, the term "mirror" does not appear in Claims 47- 61, 80-91, 108-109,111-118,132-133. Therefore applicants disagree with the Examiner's conclusion "Therefore, the first electrode would have to be some electrode below the pixel."

The Examiner further states "The electrodes below the pixel are not shown in the specification or the figures to have the transistor below them. "Since the claims do not use the language "electrodes below the pixel", applicants are not sure what the Examiner is referring to. Applicants request that the Examiner specifically point to claim language so that they can respond to the Examiner's comments.

The Examiner further states "Although the transistor must be in the semiconductor layer, it need not be below any of the layers connecting the pixel to the transistor itself." Applicants teach an example wherein the transistor is below the pixel as described above.

The Examiner further states:

> Further, most of the layers construable as the first electrode lack an absorbing layer below them, or an element which can be considered a "frame" around them. and particularly not an opaque frame. To be a frame, a material would have to be located so as to be a border for the first electrode. No layer is shown doing this. All of the layer overlap the pixel substantially, and therefore do not border the pixel electrode. The same is true of the layers in relation to the electrode 22. The insulating layers and such run above and below it; they have no edge bordering the electrode and substantially framing it. Please note Appendix 11 which shows the definition of "frame" as being "an open structure or rim for encasing, holding or bordering" (noun), or "to enclose as in or as if in a frame, such as to frame of a painting" (verb).

Applicant respectfully disagrees with the Examiner's comments. Applicant teaches at Col. 3, lines 8-11:

> A reflector/absorber layer 34 functions to block or attenuate ambient light and impinging light on spatial light modulator 10 and passing through openings or gaps 56 between mirrors such as bottom electrode/mirror 33.

Thus applicants teach a layer that absorbs. Layer 34 is below electrode layer 33 as shown in applicants' Fig. 1. US 5652667 to Kurogane teaches at Col. 4, lines, 23-25:

> The edge of the pixel electrode 2, which is a frame 21, is filled up with a silicon dioxide insulating film.

Applicants teach at Col. 3, lines 26-31:

> Dielectric layer 46 is formed over reflector/absorber layer 34 and fills the gap between reflector/absorber layer 34 and metal layer 24 and/or electrode/mirror 30.

The applicants frame is the dielectric material 46 surrounding the edge of the metal layer 24 and/or electrode/mirror 30, which is essentially the same as US 5652667 to Kurogane.

In the passage quoted above the Examiner states "Please note Appendix 11 which shows the definition of 'frame' as being 'an open structure or rim for encasing, holding or bordering'(noun), or to enclose as in or as if in a frame, such as to frame of a painting'(verb)." Applicants dielectric layer 46 has openings for stud 17 (see Col. 3, line 1.) Thus applicants layer 46 is a frame since the material is located so as to be a border for electrode 33.

Claims 47- 61, 74, 80-91, 107, 108-109, 111-118, 132-133 have been "rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not

described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention." Applicants respectfully disagree.

The Examiner states:

> The combination of a mirror with the **first electrode over the switching device and the capacitor,** and any reference to a frame in respect to the first electrode, or a blocking layer below it. The specification shows a single pixel electrode as the mirror, which means that the pixel electrode cannot be construed as the first electrode, as it is already recited in the claims as the mirror. Therefore, the first electrode would have to be some electrode below the pixel. The electrodes below the pixel are not shown in the specification or the figures to have the transistor below them. Although the transistor must be in the semiconductor layer, it need not be below any of the layers connecting the pixel to the transistor itself). Further, most of the layers construable as the first electrode lack an absorbing layer below them, or an element which can be considered a "frame" around them, and particularly not an opaque frame.

Applicants respectfully disagrees for the reasons given above.

The Examiner further states:

> As there is no written description of the claimed structure, on of ordinary skill could not make or use the invention, as how the layers would be constructed or formed could not be determined.

Applicants respectfully disagree for the reasons given above.

Claims 1-13, 46-52, 56-60, 62-64, 66-70, 63-74, 77-109, 113-115, 123, 127-131 have been rejected under 35 U.S.C. 112, second paragraph, "as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention." Applicants respectfully disagree.

The Examiner states:

> Regarding claims 74, 77, 104, 107, 127-131. The phrase rejection characteristic as used in the claim herein is indefinite- as what can be construed as a different reflection characteristic can be anything or some set of characteristics or profile of how light reflects off a layer. As applicant's specification does not give guidance as to what kinds of characteristics can meet this, this language is indefinite. For example, any two layers of different materials, or the same materials with different thickness or different deposition techniques has different reflection characteristics- so either anything automatically meets this (a sort of a null interpretation), or the specification gives some guidance as to what is meant so that some reasonable lines can be drawn. Here as the specification gives no guidance, the meaning of the term could be from the null interpretation to absolutely. This is not the case with Miyawaki, which the different characteristic is the reflection distribution as caused by a surface roughness or other related technique. For examination purposes, please note that the null definition is assumed; which is a different meaning than applicable for the Miyawaki reference.

Applicants' claim 74 recites:

> "A display unit according to claims 73, 75 or 76, wherein said shading layer reflects light to a different direction from said reflection electrodes to exhibit a different reflection characteristic."

Applicants' claim 77 recites:

> "said shading layer exhibits a different reflection characteristic from said reflection electrodes, said shading layer comprises an anti-reflection surface"

Applicants' claim 104 recites:

> "A display unit according to anyone of claims 103, 105 or 107, wherein said shading layer reflects light to a different direction from said reflection electrodes to exhibit a different reflection characteristic."

Applicants' claim 107 recites:

> "wherein said shading layer exhibits a different reflection characteristic from said reflection electrodes, said shading layer substantially prevents radiant energy incident on said non conductive optical blocking layer at a non-orthogonal angle from passing into said semiconductor substrate."

Claims 108 and 109 do not recite "reflection characteristics".

Applicants' claim 127 -131 recites:

> "wherein said shading layer exhibits a different reflection characteristic from said reflection electrodes."

Applicants teaches at Col. 3, lines 51-65:

> With the structure shown in FIG. 1, shielding the semiconductor devices in substrate 14 forming electrical circuits 16 from light is accomplished by the combination of electrode/mirror 30, and reflector/absorber layer 34. Both the electrode/mirror 30 and reflector/absorber layer 34 are sufficiently thick so that they are optically opaque. Light or radiant energy 54 and 58 incident in opening 56 between electrode/mirrors 30 and 33 (partially shown on the left side of 30 in FIG. 1 of liquid crystal device 12 and the adjacent liquid crystal device would enter dielectric layer 46 and would require multiple reflections as shown by arrow 59 between top surface 55 of reflector/absorber layer 34 and the bottom surface of electrode/mirror 30 to reach dielectric layers 44, 42, 40, and 36 and semiconductor substrate 14 containing electrical circuits 16 (not shown).

The first sentence of the abstract teaches:

> "A reflective spatial light modulator array is described incorporating: liquid crystal devices, mirrors, a semiconductor substrate, electrical circuits, and a reflector/absorber layer for blocking light."

Applicant teaches at Col. 3, lines 8-11:

> A reflector/absorber layer 34 functions to block or attenuate ambient light and impinging light on spatial light modulator 10 and passing through openings or gaps 56 between mirrors such as bottom electrode/mirror 33 and bottom electrode mirror 30 shown by arrows 54, 58 and 59 from passing into semiconductor substrate 14.

Applicants' teach at Col. 7, lines 39-49:

> The reflector/absorber layer 34 is formed by sputter deposition of 10 nm Ti, 100 nm Al(Cu), and 50 nm TiN and patterning by reactive ion etching (RIE). The bottom Ti layer 92 which is part of layer 34 shown in FIG. 7 is used for improved adhesion and contact resistance, a top or surface TiN layer 94 which is part of layer 34 shown in FIG. 7 is used as an antireflection coating, the bulk of the metallization is Al(Cu) layer 93 and metal layers 92-94 are patterned by RIE. TiN layer 94 is provided on the Al(Cu) layer 93 to reduce reflections so that fine features can be patterned by photolithography.

It is clear that Applicants' terminology "reflection Characteristics" is definite.

The Examiner further states:

> Regarding claims 1, 48-50, 56-60, 62-64, 66-70, 77. The term antireflection surface is indefinite. An antireflection layer has an art established meaning as a stack of dielectric layers using optical wavelength thicknesses and appropriate indexes of refraction to reduce the reflection at an interface between two layers of differing refractive indexes. This is not taught in the instant specification with regard to the layers to which the limitation claimed. Further, whereas the term antireflection film or layer has an art established meaning, but an antireflection surface does not. As the specification gives provided no definition for the term and gives no guidance as to how the language is to be construed, and as the language implies structure clearly not disclosed in the specification (an antireflection film), this limitation is indefinite. For examining purposes, it is assumed that any layer or surface which does not reflect all of the light meets this criteria, and as all surfaces absorb some light, this limitation is met by any layer not held as new matter.

Applicants respectfully disagree that the term "anitireflection surface" is indefinite. However, to further prosecution this term in these claims has been changed to "antireflection coating" support for which is found in Applicants' teaching at Col. 7, lines 39-49:

> The reflector/absorber layer 34 is formed by sputter deposition of 10 nm Ti, 100 nm Al(Cu), and 50 nm TiN and patterning by reactive ion etching (RIE). The bottom Ti layer 92 which is part of layer 34 shown in FIG. 7 is used for improved adhesion and contact resistance, a top or surface TiN layer 94 which is part of layer 34 shown in FIG. 7 is used as an antireflection coating, the bulk of the metallization is Al(Cu) layer 93 and metal layers 92-94 are patterned by RIE. TiN layer 94 is provided on the Al(Cu) layer 93 to reduce reflections so that fine features can be patterned by photolithography.

The Examiner further states:

> Regarding claims 47, 48-52, 57, 60, 63, 81-84, 87-88, 90, 113, 115. The term frame as used in the claims of this application is indefinite. Nothing in the specification looks like a frame- a frame goes around the edge (like a frame), and the specification does not illuminate the use of the term. Applicants first electrode, if considered as the post, does not have the capacitor below it and there is another element between the edge of the post and the blocking layer. If considered the pixel/mirror, the layer that would be the frame is below it, not around it. Therefore what is meant cannot be ascertained and the claims are indefinite.

Applicants respectfully disagree. As stated above the edge of an electrode disposed to overlap an opening in reflector absorber layer 34 is a frame.

The Examiner further states:

> Regarding claims 1-13, 46, 110. The term reflector/absorber is indefinite- Does this mean reflecting and absorbing (which everything does), or does it mean a reflector or and absorber? Or does it mean somewhere in between at some particular dividing line. As we don't know what the criteria is to meet this limitation, it is indefinite. For

examination purposes, it is presumed to mean anything that absorbs or transmits.

Applicants respectfully disagree. The Examiner has not responded to applicants' comments on this matter in applicants' prior response which are:

> The Examiner considers the term "reflector/absorber" indefinite. Applicants respectfully disagree and so does the USPTO since the issued parent application of the present invention, US 5,706,067 and the issued CIP application of US 6,424,388 of the present application uses this terminology in the issued claims. Moreover, the terminology "reflector/absorber" is recited in the claims of US Patent 4,312,326; 5,457,532 and 4,701,298 and is, therefore, considered definite by the USPTO. The present specification extensively uses the terminology "reflector/absorber" and its meaning is thus definite.

The Examiner further states:

> Regarding claims 78-109, 123. The language "Substantially prevents radiant energy incident on said shielding layer at a non-orthogonal angle from passing" is indefinite, as we don't know and cannot reasonably ascertain the level of blocking required to meet @4 substantially". Any of the devices, particularly Sato, would block anywhere from some to much of the light that is off normal. Does this therefore meet the limitation or not?

The terminology "substantially" is explicitly approved as definite by the MPEP at Section 2173.05(b) Relative Terminology - 2100 Patentability which states:

> **D. "Substantially"**
>
> The term "substantially" is often used in conjunction with another term to describe a particular characteristic of the claimed invention. It is a broad term. In re Nehrenberg, 280 F.2d 161, 126 USPQ 383 (CCPA 1960). The court held that the limitation "to substantially increase the efficiency of the compound as a copper extractant" was definite in view of the general guidelines contained in the specification. In re Mattison, 509 F.2d 563, 184 USPQ 484 (CCPA 1975). The court held that the limitation "which produces substantially equal E and H plane illumination patterns" was definite because one of ordinary skill in the art would know what was meant by "substantially equal." Andrew

Corp. v. Gabriel Electronics, 847 F.2d 819, 6 USPQ2d 2010 (Fed. Cir. 1988).

The Examiner further states:

> **Regarding claim 110**. The language "light blocking region" is indefinite, as there is no way to determine what constitutes a light blocking region (light blocking elements and layer are defined, as an element can block light- but a region itself is incapable of blocking light- an element of some form is required.

Applicants respectfully disagree. Claim 110 does not recite "light blocking region". Claim 110 recites:

> said reflector/absorber layer having an edge overlapping an edge of said mirror to form an overlapping region to decrease ambient light from passing into said semiconductor substrate.

Claims 1-11 and 13, 46, 61-63, 66-72, 74-75, 77-78, 92-93, 96-102, 104-105, 110, 117, 119-120, 122-130 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Sato et al., U.S. Patent #5,461,501.

The Examiner states:

> **The affidavit or declaration filed 4/5/00 under 37 CFR 1.131 has been considered but is ineffective to overcome the references,** The evidence submitted is insufficient to establish applicant's alleged actual reduction to practice of the invention in this country or a NAFTA or WTO member country prior to the effective date of the Sato reference. The evidence submitted has established conception prior to the date of the reference, however has only alleged reduction to practice prior to the reference date. Reduction to practice is the making of a device which works for its intended purpose. No evidence has been provided that such a device was fabricated or how it performed. Therefore, the evidence fails to establish that a reduction to practice occurred prior to the date of the reference(s). A general allegation that the invention was completed prior to the date of the reference is not sufficient. Ex parte Saunders, 1883 C.D. 23, 23 O.G. 1224 (Comm' r Pat. 1883). See MPEP 715. 07 **"Facts and Documentary Evid nce".**

> The evidence submitted is insufficient to establish diligence from a date prior to the date of reduction to practice of the Sato reference to either a constructive reduction to practice or an actual reduction to practice. No information relating to diligence has been provided. As no evidence was provided to establish a reduction to practice as discussed above, diligence would need to be established from just prior to the date of the reference to the filing date of the earliest of the parent applications. No information regarding the activities during that time period towards the reduction to practice or a constructive reduction to practice have been presented. Therefore, applicant has not established facts which show diligence during that time period. Where conception occurs prior to the date of the reference, but reduction to practice is afterward, it is not enough merely to allege that applicant or patent owner had been diligent. Ex parte Hunter, 1889 C.D. 218,1 49 O.G. 733 (Comm'r Pat. 1889). Rather, applicant must show evidence of facts establishing diligence. See MPEP 715.07(a) "Diligence".

Applicants respectfully disagree. The invention disclosure attached to Applicants Affidavit states in the top paragraph of page 4 thereof "Structures have been fabricated to demonstrate the efficacy of the lithography method described above." Thus Applicants have reduced to practice, prior to the filing date of US 5,461,501 to Sato et al., the specific embodiment of the light barrier structure as described in Applicants' specification. Thus Sato et al. is not a reference against the rejected claims.

Claim Rejections - 35 USC § 103

Claims 1-11, 13, 61-63, 66-72, 74-75, 78, 92-93, 96-102, 104-105, 110, 119-120 and 122-126 have been rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-13 and 26 of U.S. Patent No. 6424388.

Claims 47-55, 56-61, 80-81, 84-91, 108-109, 111-118 and 132-133 have been rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 14-18 and 22-24 of U.S. Patent No. 6424388.

Claims 48, 50-52, 57, 60, 80-84, 87, 90, 111-113, 115 and 118 have been rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 19-21 of U.S. Patent No. 6424388.

Enclosed herewith is a terminal disclaimer over US 4624388.

Allowable Subject Matter

Applicants' gratefully acknowledge the indication of allowable subject matter. Claims 12, 14, 64-65, 73, 76, 94-95, 103, 106 and 121.

In view of the changes to the claims and the remarks herein, the Examiner is respectfully requested to reconsider the above-identified application. If the Examiner wishes to discuss the application further, or if additional information would be required, the undersigned will cooperate fully to assist in the prosecution of this application.

Please charge any fee necessary to enter this paper and any previous paper to deposit account 09-0468.

If the above-identified Examiner's Action is a final Action, and if the above-identified application will be abandoned without further action by applicants, applicants file a Notice of Appeal to the Board of Appeals and Interferences appealing the final rejection of the claims in the above-identified Examiner's Action. Please charge deposit account 09-0468 any fee necessary to enter such Notice of Appeal.

In the event that this amendment does not result in allowance of all such claims, the undersigned attorney respectfully requests a telephone interview at the Examiner's earliest convenience.

MPEP 713.01 states in part as follows:

Where the response to a first complete action includes a request for an interview or a telephone consultation to be initiated by the examiner, ... the examiner, as soon as he or she has considered the effect of the response, should grant such request if it appears that the interview or consultation would result in expediting the case to a final action.

Respectfully submitted,

By: _____
Dr. Daniel P. Morris, Esq.
Reg. No. 32,053
Phone No. (914) 945-3217

IBM Corporation
Intellectual Property Law Dept.
P. O. Box 218
Yorktown Heights, New York 10598